

AMENDMENT AND RESPONSE

Serial No.: 10/668,752

Filing Date: September 23, 2003

Title: METHODS TO CONTROL THE DROOP WHEN POWERING DUAL MODE PROCESSORS AND ASSOCIATED CIRCUITS

PAGE 2

RECEIVED

CENTRAL FAX CENTER

JUN 29 2004

OFFICIAL

Amendments to the Specification:

Please amend the second paragraph starting on line 13 of page 2 as follows:

The Fig. 1 illustrates one known method of implementing droop in the DC/DC converter. The converter 10 includes a DC source V_{IN} that is selectively coupled to a power switch 14. The switch 14 may include one or more power devices in the form of a bridge. The output current I_O is connected (???) to the load R_L via an inductor 24 and a capacitor 26. The output current is sensed as current I_{CS} and is connected (???) to a current gain circuit 30. The output of the current gain circuit is the current I_{DROOP} . It is coupled to a node 36 at one input of the error amplifier 50. Also connected to node 36 is resistor R_1 and RC feedback circuit of C_{COMP} and R_{COMP} . The other input to the error amplifier is provided by the digital to analog converter (DAC) 40 and buffer amplifier 42. They set the reference voltage for the error amplifier 50. The output of the error amplifier is connected to one input of a comparator 60. Its other input receives a ramp signal. The output of the comparator is connected to a latch 18 that is controlled by a clock signal CLK. The output latch 18 controls the operation of the power switch 14 to turn the DC power on and off.